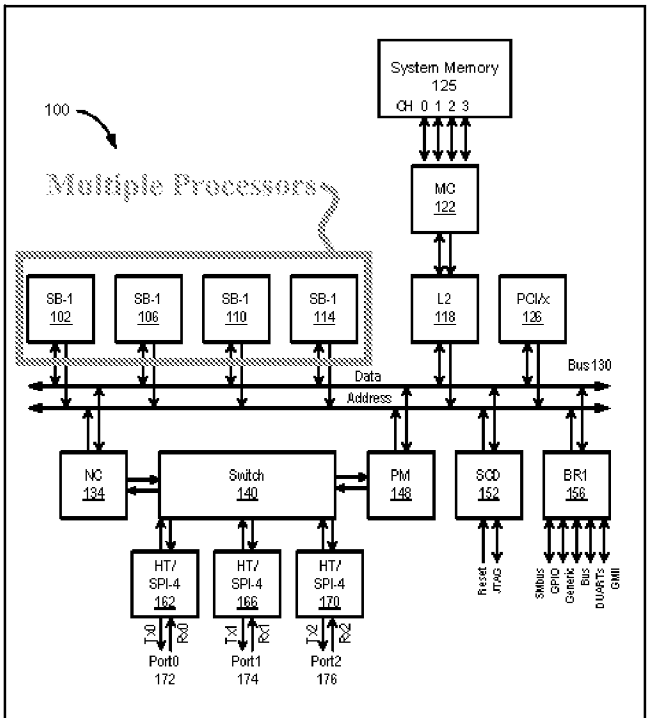
REMARKS

Claims 1-20 are currently pending. In the September 20, 2007 Office Action, the Examiner withdrew the objection to claim 7, but maintained the rejection of claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,099,325 to Kaniz et al. ("Kaniz"), and also maintained the rejection of claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Kaniz in view of U.S. Patent Publication No. 20040122973 to Keck et al. ("Keck"). In addition, the Examiner indicated that claims 4, 5, 11, 16, and 19 would be allowable if rewritten in independent form. While Applicants appreciate the Examiner's indication of allowable subject matter and reserve the right to amend the claims as suggested by the Examiner, Applicants respectfully traverse the rejections for the reasons set forth hereinbelow.

A. Claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 Are Not Anticipated by Kaniz

1. The "Multiprocessor Switching Chip" Requirement of Claims 1-13 Is Not Met By Kaniz

In response to the Examiner's previous rejection of claims 1-3, 6, 8-10 and 12-13 as being anticipated by Kaniz, Applicants explained why Kaniz failed to disclose the present invention's "multiprocessor switching chip." In particular and as shown in the annotated copy of Figure 1, Applicants have claimed a "multiprocessor switching chip" that uses a routing circuit to select one of a "plurality of destination modules within the multiprocessor switching chip" for a received packet. *See, e.g.*, claims 1 and 6 ("the routing signal is encoded in the form of an output virtual channel that is used by the multiprocessor switching chip to route packets to destination modules on the multiprocessor switching chip") (emphasis added). The "multiprocessor switching chip" is described in the application with reference to Figure 1 (plurality of processing units



Application, Figure 1

102, 106, 110, 114), Figure 2 (CPUs 260-264), and Figure 3 (CPUs 342, 344) and the associated description.

In the Final Office Action, the Examiner responds with the assertion that “Kaniz discloses a multiport switch (*a multiprocessor switching chip*) forwarding (*routing*) a packet to one of transmitter ports (*one of plurality of destination modules*) in the multiport switch with the help of internal rules checker (IRC).” *See*, Final Office Action, p. 8. With all due respect, the Examiner’s analysis completely mischaracterizes the disclosure of Kaniz. **In short, a “port” is not a “processor.”** Nor would a person skilled in the art understand that “multiport” refers to “multiprocessor.” Indeed, the claimed “multiprocessor” requirement is wholly missing from Kaniz, which instead discloses an Internal Rules Checker (IRC) 245 without in any way disclosing or suggesting that the IRC is a ***multiprocessor*** device. Kaniz Patent, col. 4, lines 57-67. As a result, the Kaniz disclosure of a “multiport switch” does not meet the claim requirement of a “multiprocessor switching chip.”

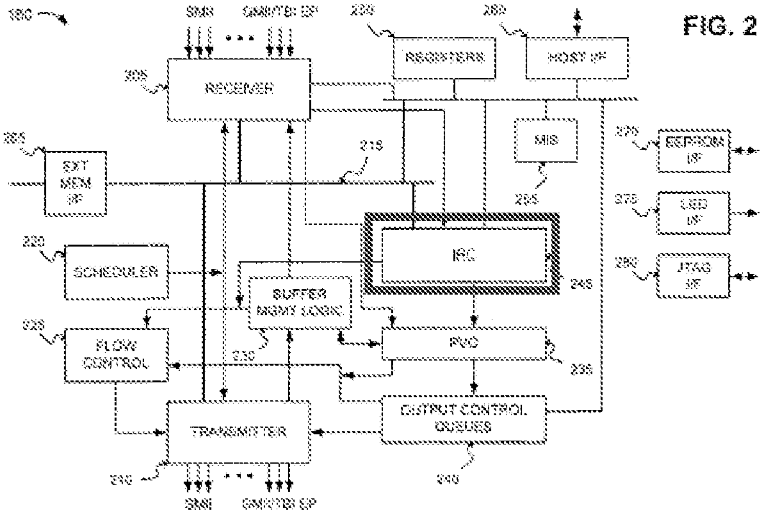


FIG. 2

Kaniz Patent, Figure 2

2. The Requirement in Claims 1-19 Of Routing Packets To Destinations In The (Multi)Processor Circuit Is Not Met By Kaniz

Another problem with the Final Office Action is that the Examiner’s analysis ignores the claim requirement that the routing circuit is used to select one of the “plurality of destination modules within the multiprocessor switching chip.” *See, e.g.*, claims 1 and 6 (“the routing signal is encoded in the form of an output virtual channel that is used by the multiprocessor switching chip to route packets to destination modules on the multiprocessor switching chip”) (emphasis added) and claim 14 (“routing a packet to one of a plurality of destinations in a processor circuit” and “transferring the first packet to a destination in the processor circuit identified by the routing result”). In contrast, the Examiner’s analysis refers only to forwarding a packet to “one of transmitter ports (*one of plurality of destination modules*).” In short, a “transmitter port” is not a destination module "within the multiprocessor switching chip" and is not otherwise a destination "in a processor circuit." As a result, the Kaniz disclosure of routing packets to "transmitter ports" does not meet the claim requirement of routing packets by selecting a destination module from "a plurality of destination modules within the multiprocessor switching chip."

3. The Requirement in Claim 20 Of Routing Packets On Virtual Channels Is Not Met By Kaniz

In response to the Examiner's previous rejection of claim 20 as being anticipated by Kaniz, Applicants explained why Kaniz failed to disclose the using extracted "input virtual channel information" to route a packet to "an output virtual channel" in the course of routing packet data. In particular, Applicants explained that disclosed multiport switch from Kaniz does not meet the requirement of "routing packet data extracted from a packet received on an input virtual channel to an output virtual channel," as recited in claim 20. In the Final Office Action, the Examiner responds with the assertion that "the above claim limitation is not recited in the claim 20" (Final Office Action, p. 8) and then asserts that "Kaniz implicitly discloses switching a packet received from an input port to a destination port via a channel" (Final Office Action, p. 9). With all due respect, claim 20 explicitly recites using extracted "input virtual channel information" to route a packet to "an output virtual channel" with the recitation that the extracted "packet data and input virtual channel information" from a received packet is used with a rule table, path table and routing table to output an output virtual channel. As indicated previously, there is simply no reference in the cited Kaniz passages to any "virtual channel," much less routing packet data "received on an input virtual channel to an output virtual channel." This is readily confirmed by the Examiner's statement at page 9 of the Final Office Action -- "Kaniz implicitly discloses switching a packet received from an input port to a destination port via a channel" – which refers only to port switching, and nowhere refers to any "virtual" channel routing.

And while not entirely clear from the Examiner's reference to an "implicit" disclosure by Kaniz, if the Examiner is asserting that Kaniz inherently discloses the claim requirements, Applicants respectfully traverse such an assertion. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." MPEP § 2112. Accordingly, Applicants request that the Examiner make the required MPEP § 2112 showing to support relying on any inherent disclosure.

In view of Kaniz's failure to meet the various requirements of the claimed invention such as recited above, Applicants respectfully submit that the Examiner has incorrectly applied the legal requirements for establishing anticipation by the Kaniz reference. To establish a *prima facie* case of anticipation, the Examiner has the burden of pointing out where each and every element of the claimed invention, arranged as required by the claims, are found in the Kaniz reference, either expressly or under the principles of inherency. *See generally*, In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986); Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). This the Examiner has not done. At best, the cited passages from Kaniz disclose a multiport switch for selectively forwarding received packets to transmitter ports, but in no way disclose or suggest Applicant's invention of a multiprocessor switch for routing packets to destinations within the multiprocessor switch, such as by routing packet data extracted from a packet received on an input virtual channel to an output virtual channel. Because a *prima facie* case has not been established that Kaniz meets or suggests the requirements of the claims, Applicants respectfully request that the anticipation rejection of claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 be withdrawn and that the claims be allowed.

B. Claim 7 Is Not Obvious Over Kaniz in view of Keck

In addition to the reasons previously set forth in response to the Examiner's rejection of claim 7, Applicants respectfully submit that the missing requirements of claim 1 discussed above are not remedied by the disclosure of Keck, and accordingly request reconsideration and withdrawal of the rejection of claim 7.

CONCLUSION

In view of the remarks set forth herein, Applicants respectfully submit that all pending claims are in condition for allowance and request that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

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Respectfully submitted,

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